CLAIMS

1. A circuit structure for a serial ATA external physical layer comprising:

a decoder/encoder connected to a storage medium controller via a set of parallel signal transmission lines and a set of parallel signal receiving lines for decoding a parallel transmission signal originated from said storage medium controller into a parallel transmission data signal and at least one control signals;

at least one serializer/deserializer connected to said decoder/encoder for the conversion of said parallel transmission data signal into a serial transmission data signal;

at least one phase locked loop connected to said decoder/encoder and said serializer/deserializer, respectively, for receiving said control signals originated form said decoder/encoder, as well as generating clock signals required for the operation of said physical layer and transmitting a reference clock signal to said storage medium controller;

at least one transmitters, connected to said serializer/deserializer, each of said transmitters being used to transmit said serial transmission data signal to a serial ATA device connected thereto via a set of serial signal transmission lines;

at least one receivers connected to said serializer/deserializer, each of said receivers being used to transmit a serial receiving data signal received from said serial ATA device connected thereto to said serializer/deserializer, and then said serial receiving data signal being converted into a parallel receiving data signal by said serializer/deserializer for transmitting said decoder/encoder; and

at least one OOB signal detectors connected to receiving signal lines of said corresponding receivers, respectively, for detecting the operation condition of said serial ATA device and transmitting at least one sets of detected status signals to said decoder/encoder, said parallel receiving data signal and said status signals then being encoded into a parallel receiving signal by said decoder/encoder and, afterward, transmitted to said storage medium controller via said set of parallel signal receiving lines.

2. The circuit structure according to Claim 1, wherein said decoder/encoder comprise a decoder and an encoder, said decoder being connected to said storage medium controller via said set of parallel signal transmission lines, and said encoder being connected to said storage medium controller via said set of parallel signal receiving lines.

3. The circuit structure according to Claim 1, wherein said serializer/deserializer comprises at least one serializers and at least one deserializers.

4. The circuit structure according to Claim 3, wherein a elastic buffer is provided

between each of said deserializers and said decoder/encoder.

5. The circuit structure according to Claim 1, wherein said phase locked loop comprises at least one transmission phase locked loop and at least one receiving phase locked loop.

6. The circuit structure according to Claim 1, wherein said control signals comprise reset signals, power control signals, transmission valid signals, and one of the combinations thereof.

7. The circuit structure according to Claim 6, wherein said control signals further comprise control signals and receiving rate control signals.

8. The circuit structure according to Claim 1, wherein said status signals comprise communication initialization signals, communication wake up signals, receiving squelch signals, receiving phase lock loop ready signals, and one of the combinations thereof.

9. The circuit structure according to Claim 1, wherein said phase locked loop has a function of transmission rate switching.

10. The circuit structure according to Claim 1, further comprising a power controller for controlling the reset and other power states of said physical layer and connected devices.

11. The circuit structure according to Claim 3, further comprising at least one selectors, one input of each of which being connected to said serializer, the other input thereof being connected to said receiver, and an output thereof may be connected to said deserializer.

12. The circuit structure according to Claim 1, wherein said circuit structure is capable of integrated into a chip.

13. The circuit structure according to Claim 1, wherein only one IDE bus is needed for connecting to said storage medium controller.

14. A signal encoding method for a serial ATA external physical layer applying to data signal transmission between said serial ATA external physical layer and a storage medium controller, essentially providing at least six continuous 6 bits of all 0's as an identification symbol for encoding, in 10-bit parallel signals during the data conversion process, in order for encoding various control signals and status signals into data signals to be transmitted.

15. The signal encoding method according to Claim 14, wherein said identification symbol of at least six continuous 6 bits of all 0's is replaced by that of at least six continuous 6 bits of all 1's.

16. The signal encoding method according to Claim 14, wherein said identification symbol is placed at the front end of said 10 bits.

17. The signal encoding method according to Claim 14, wherein said identification

symbol is placed at the tail end of said 10 bits.

18. The signal encoding method according to Claim 14, wherein said identification symbol is placed between the first one and the last one of said 10 bits.

19. A signal encoding method for a serial ATA external physical layer applying to data signal transmission between said serial ATA external physical layer and a storage medium controller, essentially providing signals, other than conversion requirement of 8 bits and 10 bits, as codes for various control signals and various status signals, in 10-bit parallel signals during the data conversion process.